GENERAL REMARKS

Office Action A allowed all 34 claims of original Application pending revision of language in the abstract and claim **4**. Amendment A provided the indicated revisions. Office Action B objected to the revision format, which did not include new material underlined and old material struck through. Amendment B provided the revisions in the correct format. All of this was in mid-2003.

After loss of Amendment B by PTO in 2003, a Notice of Forcible Abandonment was mailed to Applicant. Applicant spoke by phone with PTO attorney Patricia Ball in late 2003, and mailed per her instructions proof of Amendment B mailing and a request to revive the Application. This was also lost by PTO, which Applicant did not discover until late 2004. Applicant then filed a second petition to withdraw abandonment, which PTO acted upon only after several months and direct contact of Applicant to division director. PTO's action was to re-open case and produce Office Action C, to which the current Amendment C responds.

Office Action C, of August 15, 2005, reversed claim allowances of Office Action A, rejecting claims **1-7** and **9-34** and objecting to claim **8**.

The rejections and objections of Office Action C fell into three basic categories:

- Claims **2** and **12-18** were rejected under 35 USC SS 112 first paragraph on grounds that one skilled in the art would be unable to make the invention given in the claims, specification, and drawings.

- Independent claim **1** and dependent claims **3-7, 9-11, 17-19**, independent claim **20** and dependent claims **21-26**, independent claim **27** and dependent claims **28-29** and **31**, and independent claim **32** and dependent claims **33-34** were rejected under 35 USC 102(b) as anticipated by Hotta et al. (US patent 4,381,495).

- Independent claim **30** was rejected under 35 USC SS 103(a) as unpatentable over Hotta et al. (US patent 4,381,495) in view of Sakuragi (US patent 6,542,105).

Office Action C indicated, on page 10, that claim **8** would be allowable after rewriting as an independent claim with all the limitations of its parent claims and made an ambiguous statement about allowable status of claims **2** and **12-18** after 35 USC SS 112 issues are answered by Applicant.

With respect to Office Action C, Applicant will make detailed discussion of the numbered paragraphs presenting PTO reasoning for rejections and objections. However, Applicant's overall summary is as follows:

- Regarding 35 USC SS 112 rejections of claims **2** and **12-18**:
  - 35 USC SS 112 first paragraph rejection of claim **2** in Office Action C numbered paragraph 4 relies on lack of enablement for a circuit which is well-known in the prior art and reasonably presumed by the Applicant to be well within the knowledge of a skilled practitioner of the art.
  - 35 USC SS 112 first paragraph rejection of claims **12-18** in Office Action C numbered paragraph 4 relies lack of enablement for an element which does not appear in the claims.
  - Further 35 USC SS 112 first paragraph rejection of claims **12** and **17** and their dependent claims **13-16** and **18** in Office Action C numbered paragraphs 5-7 is unwarranted because the cited unclear material is in fact discussed in detail in the specification.

- Regarding 35 USC 102(b) rejections citing the prior art of Hotta et al. (4,381,495):
  - Office Action C incorrectly identified certain elements in Hotta et al. as being the same as elements in the Applicant's invention for independent claims **1**, **20**, and **32**, when in fact Hotta et al. fails to have all the limitations in each of these claims and their dependent claims. This resulted in improper 35 USC 102(b) rejection of claims **1**, **3-7**, **9-11**, **19, 21-26**, and **32-34**.
  - Office Action C rejected claims **17-18** without giving any reasons. These claims are dependent claims of independent claim **1** and so should not

have been rejected since Hotta et al. fails to have all the limitations of the parent claim.

- Office Action C rejected independent claim **27** on the basis of an incomplete understanding of how the invention in Hotta et al. Fig. 1 functions. However, recognizing the broad language in original claim **27**, Applicant has amended the claim in this Office Action C so that is narrower in scope and still fully consistent with the original material in the specification and figures. Dependent claims **28** and **31** have also been amended. Hotta et al. did not, and does not, have all of the limitations of claims **27**, **28**, or **31** and the claims should not have been rejected under 35 USC 102(b).

- Regarding 35 USC 103(a) rejection of claim **30** as anticipated by Hotta et al. (4,381,495) in view of Sakuragi (6,542,105):
  - Claim **30** is dependent on claim **27**, which Hotta et al. does not anticipate.
  - Sakuragi teaches away from combination with Hotta et al.
  - Advances in semiconductor manufacturing teach away from combining the old (circa 1983) ideas of Hotta et al. with the ideas of Sakuragi (circa 2001).
  - The one combination of material from Sakuragi (one of Sakuragi's prior art figures) with Hotta et al. which has some resemblance to claim **27** lacks all the elements of narrowed claim **27**, and therefore of dependent claim **30**.

Overall, Applicant will submit that independent claim **1** and its dependent claims **2-19**, independent claim **20** and its dependent claims **21-26**, claim **27** amended, and its dependent claims **28-31** (**28** and **31** amended), and independent claim **32** and its dependent claims **33-34** should be allowed.

Applicant has also amended claims **20, 21, 24, 32** and **34** with correct references to previously cited elements.

Drawing Objection

Office Action C made the following statement on page 2:

> It is suggested to indicate the direction of the path of the signal in the drawings.

Applicant requests further clarification of this suggestion. Application has three figures, Fig. 1, Fig. 2, and Fig. 3, and in each the signal path is made clear by the combination of the figure and accompanying discussion in the specification.

A comprehensive explanation of the components and operation of the circuit of Fig. 1 appears in the section DESCRIPTION – FIGURE 1 on pages 10-12 of the original Application. A comprehensive explanation of the components and operation of the circuit of Fig. 2 appears in the section DESCRIPTION – FIGURE 2 on pages 12-13 of the Application. A comprehensive explanation of the components and operation of the circuit of Fig. 3 appears in the section DESCRIPTION – FIGURE 3 on pages 13-15 of the Application.

Beyond this, all of the parts in the figures are clearly labeled with text captions and with numeric labels which are well-defined in the section REFERENCE NUMERALS IN DRAWINGS.

Claim rejections – 35 USC SS 112

In Office Action C, numbered paragraph 3 on page 2 quoted the first paragraph of 35 USC 112. Claims **2** and **12-18** were rejected under this paragraph of the United States Code as follows:

- Numbered paragraph 4 on pages 2-3 of Office Action C rejected claims **2** and **12-18** under 35 USC SS 112 on grounds of the specification lacking enablement for an element of claim **2**.

- Numbered paragraph 5 on page 3 of Office Action C further stated that elements of claims **12** and **17** were not clear in the drawings.

- Numbered paragraph 6 on page 3 of Office Action C rejected claim **18** under 35 USC SS 112 as a dependent claim of rejected claim **17**.

- Numbered paragraph 7 on page 3 of Office Action C rejected claims **13-16** under 35 USC SS 112 as dependent claims of rejected claim **12**.

Applicant will discuss each of these points in the remainder of the 35 USC 112 sections below.

Office Action C – pp. 2-3 – paragraph 4 – 35 USC 112 paragraph 1 rejections

Office Action C paragraph 4 on pages 2-3 reads as follows:

> Claims 2 and 12-18 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "first analog reference source comprises a first current source charging a first capacitor, whereby said means for causing said first analog reference signal to change as a function of time is said first current source and whereby said first analog reference signal is a voltage across said first capacitor" as recited in claim 2, does not reasonably provide enablement for "first analog reference source comprises a first current source charging a first capacitor, whereby said means for causing said first

analog reference signal to change as a function of time is said first current source and whereby said first analog reference signal is a voltage across said first capacitor". The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to –make --, -- use---, or – make and use – the invention commensurate in scope with these claims. It is not seen in the drawings where these limitations are shown.

The cited element does not appear in claims 12-18

With respect to Office Action C, paragraph 4, claims **12-18** do not recite the element which paragraph 4 is citing as the reason for rejecting those claims under 35 USC SS 112 first paragraph.

The cited element appears in claim 2 but is well-understood from prior art

Regarding claim **2**, the element cited in Office Action C paragraph 4 is present. In the figures, the "first analog reference source" of claim **2** providing the "first analog reference signal" is depicted as a black-box "analog reference source **18**" providing "a first analog reference signal **20**".

While it is true that the figures do not depict a current source charging a capacitor to create a time-varying voltage as the analog reference signal, techniques for producing analog reference waveforms by charging capacitors are well-known in the prior art. See, for instance, column 5, lines 41-50 of cross-referenced related application of the Applicant PARALLEL AND SHARED PARALLEL ANALOG-TO-DIGITAL CONVERSION FOR DIGITAL IMAGING, issued as U.S. Patent 6,559,788 on May 6, 2003 and incorporated into the Application by reference. The paragraphs of page 5 lines 17-19 and page 9 lines 5-12 in the Application clearly reference the same material, and discussions in THE ART OF ELECTRONICS, a widely-used textbook of basic electronic circuits and circuit design.

Applicant submits that a skilled practitioner of the art would be well aware of the following:

- A current source charging a capacitor causes a voltage change, which can be up or down depending on the direction of the current.
- A constant current source charging a capacitor creates a voltage ramp across the capacitor.
- A voltage ramp is used as an analog reference signal in data conversion, specifically in single-slope A/D conversion.
- Given Applicant's discussion in the specification, a voltage ramp created by a constant current charging a capacitor would be a clear and obvious candidate for the analog reference signal in Application's claim **2**.

When it is unclear how some element of a new invention is actually constructed, detailed illustration of the element in figures is useful and perhaps even required for adequate understanding of the invention. However, when an element has exemplars which are well-understood and widely-used in the prior art, and the details of the element's internal workings are not critical to the central ideas of the new invention, a pictorial discussion should not be required. In the case of the present invention, the current-source-charging-a-capacitor elements in claim **2** fall in the latter category. Prior art and the discussion and references in the specification point to well-understood, widely-used analog waveforms and techniques for analog waveform generation. Construction of an analog waveform generator by dint of a current charging a capacitor, wherein the analog waveform is a time-varying voltage across the capacitor, is well within the knowledge and abilities of one skilled in the art of analog or mixed-signal circuit design.

Therefore, claim **2** should not be rejected under 35 USC 112 first paragraph on grounds of the limiting element cited in Office Action C numbered paragraph 4 not being enabled in the specification.

Office Action C – p. 3 – paragraph 5 – 35 USC 112 paragraph 1 rejections

Office Action C paragraph 5 on page 3 reads as follows:

> Also it is unclear where in the drawing where the "parallel DAC is implemented with a first counter and the first analog reference signal both being shared" as claimed by the applicant in claims 12, 17.

Regarding Office Action C numbered paragraph 5 and claim 12

Fig. 2 of the Application shows parallel digital-to-analog conversion implemented with a first counter and first analog reference signal both being shared. First counter **4** provides first count **6** to both first digital comparator **8** and second digital comparator **26**, and is therefore shared between two D/A converters of the invention. First analog reference source **18** provides first analog reference signal **20** to both first sample-and-hold circuit **16** and second sample-and-hold circuit **30**, and is therefore shared between the same two D/A converters of the invention. Recording of a value of first analog reference signal **20** by first sample-and-hold circuit **16** is triggered by first digital comparator **8**, thereby producing the analog output of one DAC. Recording of a value of the first analog reference signal **20** by second sample-and-hold circuit **30** is triggered by second digital comparator **26**, thereby producing the analog output of the second DAC.

A similar discussion with further details appears in the Specification in the section DESCRIPTION-FIGURE 2 on pages 12-13.

Regarding Office Action numbered paragraph 5 and claim 17

Claim **17** in fact does not make reference to "parallel DAC...implemented with a first counter and the first analog reference signal both being shared", contrary to the assertion in Office Action C numbered paragraph 5. Claim **17** enumerates two analog reference sources and only that "parallel digital-to-analog conversion is implemented with [a] first counter being shared".

None of the three figures in the Application in fact shows parallel D/A conversion with two separate analog reference sources and a shared counter. However, it is clear from the figures how this could be implemented. The basic required components of the D/A converter of the invention are in Fig. 1. Fig. 2 shows an embodiment with counter **4** and first analog reference source **18** shared in two parallel D/A converters. Fig. 3 shows an embodiment with first analog reference source **18** shared but separate counters in two parallel D/A converters. Implementing an embodiment with two separate reference sources and a shared counter could obviously be accomplished by adding a second analog reference source to Fig. 2 and using it in place of first analog reference source **18** to provide an analog reference signal to one of the sample-and-hold circuits.

Applicant therefore submits that the elements of claim **17** not depicted in the figures, in combination with claim **17**, the figures, and the text discussion in the specification, enable one skilled in the art to implement the invention defined by claim **17**, and that claim **17** should not be rejected under the first paragraph of 35 USC 112.

Office Action C – p. 3 – par. 6 – 35 USC 112 par. 1 Rejection of Claim 18

Office Action C paragraph 6 on page 3 reads as follows:

> Claim 18 is automatically rejected due to the fact that it depends on claim 17 which is rejected under 112, 1st.

As discussed above, the material cited in Office Action C numbered paragraph 4 does not appear in claim **18** or its parent claims **17** and **1**. As discussed just above, the material cited in Office Action C paragraph 5 as unclear in the drawings and resulting in 35 USC 112 paragraph 1 rejection of claim **17** is not part of claim **17**, but elements of claim **17** which Applicant noted do not appear specifically in the drawings are clearly suggested by the claim, the specification, and the figures. Applicant submits that dependent claim **18** should not be rejected under 35 USC 112 paragraph 1.

Office Action C – p. 3 – par. 7 – 35 USC 112 par. 1 Rejection of Claims 12-16

Office Action C paragraph 7 on page 3 reads as follows:

Claims 13-16 automatically rejected due to the fact that it depends on claim 12 which is rejected under 112, 1st.

Claims **13-16** are dependent claims of claims **12** and **1**. As discussed above, the elements recited in Office Action C numbered paragraph 4 appear in claim **2** but not in claims **12-16**. As also discussed above, Fig. 2 and the corresponding discussion in the specification make clear the material in claim **12** recited in Office Action C numbered paragraph 5 as being unclear. Applicant therefore submits that dependent claims **13-16** should not be rejected under 35 USC 112 first paragraph.

Claim Rejections – 35 USC SS 102

In numbered paragraph 9 on page 3, Office Action C rejected claims **1, 3, 4-7, 9-11, 17-19,** and **31-34** under 35 USC 102(b) as anticipated by Hotta et al. (US patent 4,381,495). Office Action C reasoning in support of these rejections was given in numbered paragraphs 10 through 33 on pages 3-9.

The remainder of this Amendment C discussion with respect to 35 USC 102(b) claim rejections is organized as follows:

- First, Applicant summarizes and discusses the invention of Hotta et al.

- Next, Applicant discusses some general misconceptions of Office Action C about individual components in Hotta et al. and in the Application, which misconceptions underpin most of the 35 USC 102(b) rejections.

- Next, each numbered paragraph in Office Action C detailing 35 USC 102(b) rejections of claims as anticipated by Hotta et al. is addressed. For almost all the numbered paragraphs, Applicant has found that Hotta et al. does not have or suggest all of the limitations of the rejected claims, particularly of the parent claims **1**, **20**, **27**, and **32**. For some of the rejected claims Hotta et al. does not have or suggest additional dependent-claim limitations.

- Applicant notes that no supporting paragraph was given in Office Action C for rejection of claims **17** and **18** under 35 USC 102(b) as anticipated by Hotta et al.

Applicant's summary of Hotta et al. (US 4,381,495)

Prior art U.S. patent 4,381,495 entitled DIGITAL-TO-ANALOG CONVERTER WITH ERROR COMPENSATION and issued to M. Hotta, K. Maio, N. Yokozawa, and H. Nagaishi on April 26, 1983 discusses circuits for digital correction of linearity errors in a digital-to-analog converter. The filing date for the patent is October 8, 1980. Foreign application priority filing in Japan dates from October 24, 1979.

The invention of Hotta et al. is a digital-to-analog converter system with a digital-to-analog converter and additional circuitry aimed at compensating for transfer function nonlinearity. The specific novelty of Hotta et al. relative to its prior art is that it alternates between two modes – one in which it computes a digital correction term to compensate for transfer function non-linearity and one in which it acts as a regular D/A converter using the compensation terms. The net effect of this is to allow regular D/A conversion at half of the nominal conversion rate while gradually building a look-up table of the digital correction terms.

Hotta et al.'s claims are indefinite

Applicant notes that all of Hotta et al.'s claims are in fact indefinite. Hotta et al. claim **1** in column 9 lines 65-68 includes in part (b) a reference to "said analog digital converter" which renders the claim indefinite, as the only prior elements mentioned were "a digital-to-analog conversion system" and "a digital-to-analog converter". The remaining Hotta et al. claims **2-6** are also indefinite because they depend on indefinite claim **1**.

D/A converter performance measures

D/A converters are typically designed to map a set of ordered, uniformly-spaced digital number inputs to a set of ordered, uniformly-spaced analog signal outputs. To the extent that the analog output set deviates from this ideal, the transfer function of the converter is non-linear. Two performance measures which appear in D/A converter specifications are differential non-linearity (DNL) and integral non-linearity (INL). DNL measures the maximum difference between two adjacent analog outputs (corresponding to two adjacent digital inputs) relative to the ideal uniform spacing, over the full range of

inputs. INL measures the maximum deviation in the analog outputs from an imaginary ideal line, usually determined by the two endpoints of the analog range.

While the details are discussed below, the basic idea of Hotta et al. and the prior art on which it built is to identify for some digital input X another digital input (X+d) whose D/A converter output is closer to the ideal desired output than the actual output corresponding to X. Then, whenever X is to be converted, (X+d) is provided as the actual D/A converter input, yielding the more-desirable analog output. The term "d" is a digital correction, so the re-mapping can be implemented by storing a set of "d" terms in a look-up table and adding them to incoming X values.

This method can improve DNL and INL measurements, but only gross ones, since each input to be corrected can only be corrected if there is a range of other possible inputs nearby. In other words, correction can be to the precision of X less the precision of d.

Two other performance measures of D/A converters are speed and precision. Speed is measured in conversions per unit of time, usually conversions per second. Speed is typically limited by the time required to complete a single full conversion, in the case of a serial converter. A substantial amount of this time may be allocated to letting the analog output transition from an old value and settle at a new value. In fact, in Hotta et al. it is treated as the dominant component of the conversion time. Precision reflects the number of allowed inputs, and is usually measured by the number of bits in digital input numbers. A 4-bit D/A converter would have 2^4=16 allowed inputs, while an 8-bit converter would have 2^16=256 allowed inputs, and so forth.

Operational details of Hotta et al.

As mentioned above, the D/A converter of Hotta et al. operates in two modes. In one mode, digital correction terms are computed and stored in a look-up table. In the other mode, the invention functions as a regular D/A converter, with the digital inputs modified by the digital correction terms to correct for transfer function non-linearity. Regular D/A conversion occurs on a relatively short time scale. Hotta et al. gives a 5 micro-second D/A settling time in column 5 line 30, which presumably was cutting edge in the era – circa 1979 that is – of Hotta et al. On the other hand, correction of a full set of digital

corrections occurs on a relatively long time scale. Hotta et al. allow 1.3 seconds for this with the above D/A converter. See column 5 lines 31-35.

Switching between modes

Referring to Hotta et al. Fig. 1, the base component of the overall D/A converter is DAC **1**. This is depicted as having three sets of inputs provided by switch **71**, switch **72**, and switch **73**. These inputs are all digital inputs. DAC **1** has one output, which is an analog output. This is passed to switch **74**, which can route it either to sample-and-hold circuit **11** or to sample-and-hold circuit **12**. The signal SCLK from timing pulse generator **100** controls the state of all four switches.

The actual invention of Hotta et al., as noted above, is that the D/A conversion system alternates between the two modes so that regular D/A conversion can proceed while the full set of digital correction calculations is incomplete. In the simplest form, DAC **1** provides one output for a compensation term calculation, then one regular (compensated) output, then one output for a compensation term calculation, then one regular output, and so forth. See column 5 lines 38-41. DAC **1** could also provide multiple regular outputs in between each output for compensation term calculation.

Compensated regular D/A conversion mode

In regular D/A conversion mode, switch **71** passes the input UB to DAC **1**, switch **72** passes the input LB to DAC **1**, and switch **73** passes a digital correction from the OUT port of RAM **5**. Input UB represents the upper (i.e. more-significant) bits of a digital number to be converted to an analog output (see column 1, line 30). Input LB represents the lower (i.e. less-significant) bits (see column 1, line 66). UB and LB are always processed simultaneously as a single digital number. Their separation and passage through two switches serves mainly to illustrate that in digital correction calculation mode, the count from counter **6** can have fewer bits than the precision of DAC **1** and that the count bits correspond to more-significant bit values, as discussed below.

For the output in compensated regular D/A conversion mode, switch **74** passes the analog output of DAC **1** to sample-and-hold circuit **12**, where it is sampled, held, and provided as system output O/P (with a bar over the O).

While not explicitly shown, the black-box DAC **1** includes means for combining the digital correction passed via switch **73** with the digital number defined by UB and LB so that the digitally-corrected digital input is converted to the desired compensated analog output.

Computing digital correction terms

In compensation term calculation mode, switch **71** passes the count from counter **6** to DAC **1** instead of passing UB, switch **72** passes a "0" string instead of LB, and switch **73** passes a "0" string instead of a digital correction. In other words, if UB has M bits and LB has N bits, the digital inputs to (M+N)-bit D/A converter DAC **1** for computing digital correction terms are a sub-sampled set of the allowed inputs, specifically the 2^M allowed inputs whose N least-significant bits are zero. During computation of the digital correction terms, the digital correction supplied is "0", or no digital correction.

In the digital correction computation mode, members of this sub-sampled set of allowed inputs are applied to the D/A converter in an ordered fashion, alternating with one or more digital numbers for the regular compensated D/A conversion mode. The inputs for digital correction computation are applied in increasing order and are generated by counter **6**. For each one, the analog output of DAC **1** is sampled and held by sample-and-hold circuit **12**. The sampled-and-held analog signal is applied to the inverting input of an analog comparator, comparator **2**. Simultaneously, another analog signal which is an increasing voltage ramp supplied by voltage ramp generator **8** is applied to the non-inverting input of comparator **2.**

Comparator **2** compares the sampled-and-held DAC **1** analog output to the analog voltage ramp. When the ramp exceeds the sampled-and-held DAC **1** analog output, the digital output of comparator **2** triggers recording of a digital count correction. The digital count correction comes from counter **4**, which tracks elapsed time during a digital correction calculation. The digital count correction is captured by latch **51** and then written into a look-up table in RAM **5**.

Next, the mode switches to regular D/A conversion with compensation, for one or more digital input numbers, while the ramp is still rising. Then the next count value from counter **6** is provided for another digital correction computation. The count values from counter **6** are provided in increasing order because the ramp continues to rise. If a counter **6** count X and Y are provided sequentially, and Y has a corresponding DAC **1** output that is less than that that of X, comparator **2** won't trigger recording of a correct count value from counter **4** on a single ramp cycle because the voltage ramp will already have exceeded the latter sampled-and-held DAC **1** output before it is presented. The goal is to compute all of the digital corrections during one ramp rise cycle, while periodically running the system in regular mode. This is analogous to real-time processing where a longer computation is interrupted by shorter actions with higher time priorities.

Technology and time scale issues of Hotta et al.

While D/A converter speeds are up – 10 to 100 nano-second settling times being routine, as opposed to the figure in Hotta et al. being 5 micro-seconds (5000 nano-seconds), one part of the invention of Hotta et al. that hasn't seen a lot of change is voltage ramp generation.

A well-known and widely-used method for generating a voltage ramp is to charge a capacitor with a constant current. Nowadays, one might consider generating a voltage ramp using a good D/A converter. However, this isn't an approach one would combine with Hotta et al. because the invention would then be using a good D/A converter to improve a bad D/A converter. In such a case it would be better to use the good D/A converter directly.

It is today, and was in 1979, comparatively easy to build a high-quality constant current source and a capacitor. This means it is, and was, easy to build a voltage ramp. Unfortunately, in both eras, a high-quality voltage ramp requires a slow ramp rise-time. In the real world, there are no ideal capacitors. Practical capacitors exhibit parasitic resistive, inductive, and capacitive behavior. In particular, a phenomenon known as dielectric absorption limits the quality of steeply-sloped voltage ramps. Dielectric

absorption is sometimes modeled as a parasitic series resistor and capacitor in parallel with a nominally-ideal capacitor. This parasitic RC component creates a transient non-linear response whenever the current across the actual capacitor changes. From the perspective of ramp generation, a constant current is switched on at the start of ramp generation, triggering the transient. If the current is large in order to enable a fast-rising signal, the transient will be large and will last for a long time relative to the ramp duration. If the current is small, the transient will be small and will die off quickly, but the ramp won't rise quickly.

In other words, to get a highly linear voltage ramp, it's necessary to have a slow rise time.

While voltage ramp generation hasn't improved with technology advances (due to dielectric absorption) component size and matching have. It is much easier to make well-matched active and passive integrated circuit components today than it was in 1979. Today's components are also smaller. Manufacturing processes have improved, and there are formerly unavailable technologies such as laser-trimming of components and on-chip tunable components such as floating-gate MOSFETs. These improvements have enabled construction of base D/A converters (e.g. DAC **1** of Hotta et al. Fig. 1) that do not need the elaborate compensation scheme of Hotta et al. See, for instance, the data sheet for the Analog Devices AD5582/AD5583 (the URL is http://www.analog.com/UploadedFiles/Data_Sheets/32975162110307AD5582_83_a.pdf). The products are 12-bit and 10-bit parallel-input, voltage-output D/A converters, 4 to a packaged chip, with 5 micro-second settling times, worst-case INL of +/-1 LSB, and worst-case DNL of 1 LSB. The converters are based on a switched resistor ladder network architecture and don't require any additional INL or DNL compensation.

An important note about Comparator 2 in Hotta et al. Fig. 1

Many of the Office Action C rejections of claims in the Application center on a misinterpretation of comparator **2** in Hotta et al. Fig. 1.

In Hotta et al. Fig. 1, comparator **2** is depicted as having two inputs, one labeled with a "+" sign and one labeled with a "-" sign, as well as one output. The two inputs are

connected to what are clearly analog signals. The "+" input is connected to the output of ramp voltage generator **8**, and the "-" input is connected to the output of sample-and-hold circuit **12**. Meanwhile, the output is connected to what are clearly digital inputs of digital circuits – latch **51**, the S input of S-R flip-flop **3**, and an input of AND gate **31**.

The two input terminals of comparator **2** are a non-inverting input indicated by a "+" sign and an inverting input indicated by a "-" sign. When the analog signal at the non-inverting input is greater than the analog signal at the inverting input, the comparator output saturates at its highest value. When the analog signal at the non-inverting in put is less than the analog signal at the inverting input, the comparator output saturates at its lowest value. There is also a non-zero offset voltage which is unique to each comparator and which may vary with temperature and component age, so that in practice, one input must exceed the other by this offset voltage for any output transition to occur.

The output of comparator **2** does not itself record either of the analog input signals. It merely indicates which is larger at any given time, subject to the effect of the offset voltage.

The presentation and connectivity of comparator **2** are clearly consistent with it being an analog comparator with a non-inverting input "+" and an inverting input "-". In the specification of Hotta et al., all discussion of comparator **2** treats it as an analog comparator. Comparator **2** is described as a "comparator", but it is an analog comparator.

Comparator **2** in Hotta et al. Fig. 1 is not a digital comparator.

In addition to not being a digital comparator, comparator **2** is unable to perform the function of a digital comparator of detecting when one time-varying digital input sequence reaches another digital input. If two analog signals with a difference less than the offset voltage of the comparator are applied to the input terminals one way, the output will saturate high (or low), while if the two analog inputs are switched, the output will saturate low (or high). This means that the comparator has no way of comparing inputs with a quantized range of equality – in other words, digital inputs.

Applicant took care to define and use "digital comparator"

With respect to the present invention, Applicant went to great lengths in the original Application to properly define the term "digital comparator" which appears in claims, figures, and the text.

According to the Specification, a "digital comparator" accepts as inputs two digital numbers, and provides as output a digital indicator signal which indicates when the two inputs are equal. A digital comparator does not accept analog inputs, and cannot compare analog inputs. An analog comparator does not accept digital inputs, and cannot compare digital inputs.

In the claims of the Application, the term "comparator" is used by itself. It always appears as "digital comparator".

In the figures of the Application, the digital comparators always appear with an internal caption "digital comparator" and a corresponding numeric label which is identified in the REFERENCE NUMERALS IN FIGURES AND DRAWING section as a digital comparator. The outputs are properly labeled as digital outputs. The inputs are properly labeled as digital inputs, and indicated with the usual graphical convention of a slash through a single routing line.

In the specification, digital comparator functioning is carefully described. For instance, the third paragraph of page 3, on lines 12-16 states, with respect to digital comparator **8** in Application Fig. 1, the following:

> The circuitry of first digital comparator **8** determines whether first count **6** is equal to first digital number value **10**. When the two values are equal, first digital comparator output **14** triggers first sampled-and-hold circuit **16** to sample and hold the analog value of analog reference signal **20**.

Similarly, the third full paragraph on page 12, lines 20-27, describes the operation of both first digital comparator **8** and second digital comparator **26** of Application Fig. 2.

Similarly, the third full paragraph on page 14, lines 15-23 describes the operation of both first digital comparator **8** and second digital comparator **26** of Application Fig. 3.

The only place in the Application where "comparator" does not appear right after "digital" is the second full paragraph of page 4, lines 9-16. This paragraph clearly suggests a "comparator" having digital inputs and a digital output, with an analog output generated by averaging the digital output over time. The "comparator" suggested in this paragraph has an output that is high when a first digital input (digital number value) is less than a second digital input (count) and that is low when the first digital input is greater than the second digital input.

An important note about connections in Hotta et al. Fig. 1

Another issue which appears in multiple 35 USC SS 102(b) claim rejections is storage. Digital circuits can store or record digital number values – for instance, latch **51** and the memory elements in RAM **5** of Hotta et al. Fig. 1. Analog circuits are needed to store or record analog values – for instance, the sample-and-hold circuits **11** and **12** in the same figure. An analog comparator output is a digital signal and does not record the value of either input directly, though it could trigger recording of an analog signal value by a sample-and-hold circuit. However, for this to occur, the analog signal to be recorded must be passed as an input to the sample-and-hold circuit.

In a number of 35 USC 102(b) Hotta et al. rejections of Application claims, the presence of sample-and-hold circuits in Hotta et al. Fig. 1 is equated with means for recording analog signal values from the voltage ramp generator. However, without a connection passing the voltage ramp to a sample-and-hold circuit, the sample-and-hold circuit does not amount to means for recording a value of the voltage ramp.

Office Action C – pp. 3-4 – par. 10 – 35 USC 102(b) Rejection of Claim 1

Office Action C makes the following statement on pages 3-4 with respect to Application claim **1**:

> Regarding claim 1, Hotta et al. discloses a machine used for digital-to-analog conversion (fig. 1) comprising : a first counter (6) which provides a first count; a first analog reference source (8) which provides a first analog reference signal; a first digital number value (UB) to be converted to a first analog value (fig. 1); means (clock generator 9) for causing the first count to change as a function of time (the clock is in function of time); means for causing the first analog reference signal to change as a function of time (fig. 1); means (2) for detecting when the d first count reaches the first digital number value (the comparator compares the digital value with a reference number; col. 3, lines 50-56); means for recording the value of the first analog reference signal as the first analog value when the first count reaches the first digital number value whereby the first analog value is the converted value of said first digital number value (col. 4, lines 19-27; abstract).

Applicant submits the following:

- The Office Action C statement about the function of Comparator **2** in Hotta et al. Fig. 1 is incorrect.
- The Office Action C assertion of means for recording the value of the first analog reference signal being present in Hotta et al. Fig. 1 is incorrect.

Comparator 2 in Hotta et al. Fig. 1 is not a digital comparator, and Hotta et al. Fig. 1 in fact lacks means for detecting when the first digital count reaches the first number value

On page 4, lines 2-4, Office Action C states the following identifies comparator **2** in Hotta et al. Fig. 1 with the limiting element in Application claim **1** section f:

> means (2) for detecting when the d [sic] first count reaches the first digital number value (the comparator compares the digital value with a reference number; col. 3, lines 50-56);

Hotta et al. column 3, lines 50-56 read as follows:

> An output signal SH (Fig. 2, (e)) of the sample and hold circuit **12** is applied to comparator **2**, and is compared with the ramp voltage Vr (Fig. 2, (g)). In synchronism with an output (Fig. 2, (h)) of the comparator **2** at the time when the ramp voltage Vr has exceeded the output signal SH, an output (initial value: "0…0") of an m-bit counter **4** is set in a latch **51**.

Referring to Hotta et al. Fig. 1 directly, comparator **2** has a non-inverting input indicated by a "+", an inverting input indicated by a "-", and an output. When the non-inverting input is greater than the inverting input, the output saturates at a logical high state. Otherwise, the output saturates at a logical low.

The non-inverting input is connected to Vr, the analog ramp signal provided by ramp voltage generator **8**. The inverting input is connected to SH, the analog output of sample-and-hold circuit **12**, which is sampled and held from the analog output of DAC **1**. The output of comparator **2** is connected to latch **51**, to the S input of S-R flip-flop **3**, and to an input of 2-input AND gate **31**, all of which are digital connections.

Comparator **2**, therefore, clearly compares two analog input signals – Vr and SH – and provides a digital output signal indicating which is larger. Comparator **2** does not "compare the digital value [previously identified in Office Action C as Hotta et al. Fig. 1 upper byte UB] with a reference number." Simply put, comparator **2** is not a digital comparator. It is an analog comparator.

Moreover, Office Action C previously identified counter **6** in Hotta et al. Fig. 1 as providing the first count, in the portion of numbered paragraph 10 in page 3. Hotta et al. column 3 lines 50-56 indicates that an output swing of comparator **2** triggers recording of a count value from counter **4** in latch **51**.

Hotta et al. Fig. 1 lacks means for recording values of the analog reference signal

Office Action C further states in numbered paragraph 10 on page 4 that Hotta et al. Fig. 1 includes the following:

> means for recording the value of the first analog reference signal as the first analog value when the first count reaches the first digital number value whereby the first analog value is the converted value of said first digital number value (col. 4, lines 19-27; abstract);

The suggestion is that Hotta et al. Fig. 1 includes the limiting means element in Application claim **1** part g. However, this is not the case.

As is clearly shown in Fig. 1, the output of ramp voltage generator **8** – which output Office Action C previously identified as the first analog reference signal – is only provided to the non-inverting input of comparator **2**. It is not provided to any circuit which is capable of recording its value, for instance, a sample-and-hold circuit such as sample-and-hold circuit **12**.

Hotta et al. Fig. 1 lacks two important limiting elements of claim 1

Applicant therefore submits that Hotta et al. Fig. 1 lacks two important limiting elements of Application claim **1** – the "means for detecting when said first count reaches said first digital number value" of part f and the "means for recording the value of said first analog reference signal as said first analog value when said first count reaches said first digital number value" of part g, and therefore submits that claim **1** is not anticipated by Hotta et al. Fig. 1.

Regarding Hotta et al. anticipation of claims 3, 4-7, 9-11, and 17-19

In numbered paragraph 9 on page 3, Office Action C further rejected claims **3, 4-7, 9-11,** and **17-19** under 35 USC 102 (b) as anticipated by Hotta et al. (US patent 4,381,495). Specific reasons for this were given in Office Action C numbered paragraphs 11 (claim

3), 12-15 (claims **4-7**), 16-18 (claims **9-11**), and 19 (claim **19**). Note that while claims **17** and **18** were rejected under 35 USC 102(b) in Office Action C, no reasons were given.

In rejecting these claims under 35 USC 102(b), Office Action C relies principally on the fact that all the claims are dependent claims whose independent parent claim **1** was rejected. However, as Applicant has demonstrated above, Hotta et al. Fig. 1 as discussed in Office Action C fails to have all of the limitations of claim **1**. Therefore, Applicant submits that all of these dependent claims – which do have all of the limitations of claim **1** – are not anticipated by Hotta et al.

In the following sections, Applicant will discuss the particular details of the Office Action C rejections with respect to each of the claims.

Office Action C – p. 4 – par. 11 – 35 USC 102(b) Rejection of Claim 3

With respect to Office Action C numbered paragraph 11, Applicant concedes that Hotta et al. Fig.1 includes means for causing the first count to change as a function of time.

However, as indicated above, claim **3** is a dependent claim of claim **1**. Applicant therefore submits that claim **3** is not anticipated by Hotta et al since Hotta et al lacks all of the limitations of parent claim **1**.

Office Action C – p. 4 – paragraph 12 – 35 USC 102(b) Rejection of Claim 4

Office Action C asserts in numbered paragraph 12 on page 4 the following:

> Regarding claim 4, Hotta et al. discloses a machine (fig. 1) in which the first digital clock (9) has a frequency that can vary, whereby the first count need not always change at a single rate wherein high precision DAC is possible with a high frequency of the first digital clock a high rate of change of the first count and a corresponding high dynamic power consumption and low precision DAC is possible with a low frequency of the first digital clock, a low rate of change of the first count and a corresponding low dynamic power consumption (fig. 1).

Applicant notes that Hotta et al does not discuss anywhere in its specification or claims the possibility of a variable-frequency clock. It is true that with a variable speed clock in Hotta et al. Fig. 1, the count rate of the first count will vary. However, it is not clear in Hotta et al. how a fast count would enable high-precision D/A conversion while a slow count would enable low-precision D/A conversion. In Hotta et al. Fig. 1, the actual D/A conversion is carried out by a black-box D/A converter, namely DAC 1, whose precision is unrelated to the count speed.

Moreover, in keeping with the error compensation function of the remainder of the circuitry in Fig. 1, each value of the first count provided by counter **6** is used to generate a digital correction term involving sampling-and-holding of the DAC **1** output and comparing the sampled-and-held output to the voltage ramp. Counter **6** is discussed as having 4 bits, but in general if it is an N-bit counter, there are 2^N values, and the system

requires 2^N "time intervals of the compensating operations" – in other words, 2^N D/A conversions, sampling-and-holding operations, analog comparisons, and digital correction counting, and digital correction storage – in the course of a single voltage ramp. Hotta et al give a 1.3 second correction time in the paragraph of column 5 lines 22-37. It is quite easy to build a fast counter, but it is not easy to build voltage ramp that is both highly linear and with a fast rise time. This is because non-linear effects of dielectric materials at high frequency (e.g. dielectric absorption). For instance, it might not be possible to make a voltage ramp with a 0.013 second rise time that is linear to ½ LSB, with reference to the same paragraph on column 5.

So, using a faster counter **6** in Hotta et al Fig. 1 would require a faster rise time for the voltage ramp, which might not lead to better error correction if the voltage ramp is no longer sufficiently linear or if the D/A converter output no longer has time to settle. The faster counter and faster-rising voltage ramp wouldn't necessarily result in higher-precision D/A conversion, though they would reduce the time devoted to determining the digital error compensation values.

In any case, Application claim **4** is a dependent claim of independent claim **1**. Hotta et al. does not include all the limitations of claim **1**, and also does not include all the limitations of claim **4**. Applicant therefore submits that claim **4** is not anticipated by Hotta et al.

Office Action C – p. 4 – paragraph 13 – 35 USC 102(b) Rejection of Claim 5

Office Action C asserts in numbered paragraph 13 on page 4 that Hotta et al Fig.1 discloses an analog reference source which is a voltage ramp. This is true. However, as previously discussed, Hotta et al. fails to include all the limitations of claim **1**, which is the parent of dependent claim **5**. Applicant submits that since Hotta et al. fails to include all of the limitations of claim **5**, Hotta et al. does not anticipate claim **5**.

Office Action C – p. 4 – paragraph 14 – 35 USC 102(b) Rejection of Claim 6

Office Action C asserts in numbered paragraph 14 on page 4 that Hotta et al Fig. 1 "discloses a machine in which the first analog reference source (9) comprises an

operational amplifier". Applicant notes that in Fig. 1 element **9** is a clock, whereas element **8** is a voltage ramp generator previously identified in Office Action C as the analog reference source. In any case, the ramp voltage generator **8** is a black box, and the specification and claims of Hotta et al. include no elaboration on its contents.

However, as with previous claims dependent on claim **1**, claim **6** is not anticipated by Hotta et al. because Hotta et al. does not suggest or include all of the limitations of parent claim **1**.

Office Action C – pp. 4-5 – paragraph 15 – 35 USC 102(b) Rejection of Claim 7

Office Action C makes the following statement in numbered paragraph 15 on pages 4-5:

> Regarding claim 7, Hotta et al. discloses a machine (fig. 1) in which the first analog reference source comprises a first digital-to-analog converter (1), whereby said first count can be the input to the first digital-to-analog converter (fig. 1) and whereby the first analog reference source (note the output of the DAC) can be the output of the first digital-to-analog converter (fig. 1)

With respect to previous discussion for claims **1** and **2-6**, Office Action C identified ramp voltage generator **8** as the element of Hotta et al Fig. 1 corresponding to the first analog reference source of claim **1** and dependent claims. DAC **1** in Hotta et al. Fig. 1 is not a part of ramp voltage generator **8**.

The alternative interpretation of Office Action C numbered paragraph 15 is that DAC **1** corresponds to the first analog reference source of claim **1** and dependent claim **7**. This does not make sense. DAC **1** is a D/A converter. There's no point in having a time-varying analog reference source whose output is recorded as the desired first analog value when a time-varying first count reaches a first digital number value if one can simply apply the first digital number value as a reference source input and get the desired analog value as the reference source output. With the alternative interpretation of Office Action C numbered paragraph 15, at all times the first count and the first digital number value would have to be one and the same. The Applicant's invention is a type of

D/A converter – in other words, something that could fill the DAC **1** black box in Hotta et al.

In any case, Hotta et al. lacks all of the limitations of claim **1**, the parent of claim **7**, and thus lacks all the limitations of claim **7**. Applicant submits that claim **7** is not anticipated by Hotta et al.

Office Action C – p. 5 – paragraph 16 – 35 USC 102(b) Rejection of Claim 9

With numbered paragraph 16 on page 5, Office Action C continues the alternative interpretation of DAC **1** in Hotta et al being the analog reference source, though for claim **9** and parent claim **1**. Again, Hotta et al. lacks all the limitations of claim **1**, and therefore lacks all the limitations of claim **9**. Applicant submits that Hotta et al. does not anticipate claim **9**.

Office Action C – p. 5 – paragraph 17 – 35 USC 102(b) Rejection of Claim 10

Office Action C asserts in numbered paragraph 17 on page 5 that in the machine of Hotta et al Fig. 1 "the first count controls the first analog reference source, whereby said first count need not be in increasing order or decreasing order".

In fact, Hotta et al. make no such statement or implication. Hotta et al. discusses and requires that the count start at "0000" and end at "1111". With an upward ramp, there is an upward count. While not mentioned, with a downward ramp there would have to be a downward count.

Further, because of the nature of the compensation process in Hotta et al. – testing the DAC **1** output for each first count value during a single cycle of the voltage ramp – an unordered count is specifically precluded. If a digital error correction term is measured for first count 0001, and next a digital error correction term is measured for first count 0100, the system cannot compute a digital error correction term for first count values of 0010 and 0011 because the voltage ramp will have already passed the switching points of the DAC **1** outputs corresponding to 0010 and 0011. Similarly, the compensation

scheme cannot correct for DAC **1** code errors that result in a non-monotonic transfer function for the converter.

It would be possible to have an arbitrary count sequence by using multiple compensation cycles but then within each cycle the first count would have to be incrementing upward. An extreme case would be applying exactly one first count value per ramp. However, given Hotta et al's numbers, this would imply an overall look-up table calculation time of 2^N x 1.3 = 2^16 x 1.3 = 65,536 x 1.3 = 85,197 seconds. That's almost 24 hours, and clearly not acceptable!

These arguments aside, claim **10** is a dependent claim of claim **1**. As Hotta et al. does not include all the limitations of claim **1**, it does not include all the limitations of claim **10**. Applicant therefore submits that Hotta et al. does not anticipate claim **10**.

Office Action C – p. 5 – paragraph 18 – 35 USC 102(b) Rejection of Claim 11

In numbered paragraph 18 on page 5, Office Action C states:

> Regarding claim 11, Hotta et al. discloses a machine (fig. 1) in which the first count does not control the first analog reference signal, whereby the first count should be in increasing order or in decreasing order with said first analog reference signal level changing corresponding (fig. 1).

Previously, Office Action C identified two possible analog reference sources in Hotta et al. Fig. 1 – ramp voltage generator **8** and DAC **1**. Office Action C identified the first count as the count output of counter **6**.

As is clearly shown in Hotta et al. Fig. 1 and discussed in Hotta et al's specification, counter **6** controls both ramp voltage generator **8** and DAC **1**. It controls ramp voltage generator **8** by way of the output CA, which is internally generated when the count value reaches 11..11. It controls the output of DAC **1** when switch **73** passes the count as input to DAC **1**.

These arguments aside, claim **11** is a dependent claim of claim **1**. As Hotta et al. does not include all the limitations of claim **1**, it does not include all the limitations of claim **11**. Applicant therefore submits that Hotta et al. does not anticipate claim **11**.

Office Action C – 35 USC 102(b) Rejection of Claims 17 and 18

In numbered paragraph 9 on page 3, Office Action C rejected both claim **17** and claim **18** under 35 USC 102(b) as anticipated by Hotta et al. However, numbered paragraph 18 on page 5 discusses 35 USC 102(b) rejection of claim **11**, while numbered paragraph 19 on page 5 discusses 35 USC 102(b) rejection of claim **19**. Applicant is not able to find any discussion of why Office Action C rejected claims **17** and **18**.

Notwithstanding, both claims **17** and **18** have claim **1** as a parent claim. Applicant submits that Hotta et al. lacks all of the elements of claim **17** and of claim **18**, and submits that Hotta et al. therefore does not anticipate the two claims.

Office Action C – p. 5 – paragraph 19 – 35 USC 102(b) Rejection of Claim 19

In numbered paragraph 19 on page 5, Office Action C states:

> Regarding claim 19, Hotta et al. discloses a machine (fig. 1) further including means (9) for causing the first digital number value to change as a function of time, whereby the first analog value is the converted value of the first digital number value prior to its change with time, and represents the time required for the difference between the time-varying first count and the time-varying first digital number value to reach zero (fig. 1).

The suggestion in Office Action C is that element **9** in Hotta et al. Fig. 1 – namely, the clock generator – causes the first digital number value to change with time. However, previously, Office Action C identified the input UB as the first number value. When the invention of Hotta et al. Fig. 1 is operating in compensation calculation mode, UB and LB are not connected to the input of DAC **1**. Instead, the first count from counter **6** and "0" values for LB and the digital correction term are applied. So in this mode, clock generator **9** need not have any effect on UB. When the invention of Hotta et al. in Fig. 1

is operating in D/A conversion mode (i.e. after the digital correction terms have been calculated and stored), clock generator **9** again need not have any effect on UB. UB could well be the same from sample to sample. It could also be asynchronous with the compensation circuits governed by clock generator **9**. It could also have its own clock signal entirely separate from clock generator **9**. With all of these possibilities, and no explicit control of UB by clock generator **9** depicted in Hotta et al. Fig. 1 or discussed in the specification of Hotta et al, there is no suggestion that clock generator **9** causes the first digital number value to change as a function of time.

Additionally, claim **19** is the last of parent claim **1**'s dependent claims. Hotta et al. fails to have all the limitations of claim **1** and also fails to have all the limitations of claim **19**, so Applicant submits that Hotta et al. does not anticipate claim **19**.

Office Action C – pp. 5-6 – paragraph 20 – 35 USC 102(b) Rejection of Claim 20

In numbered paragraph 20 on pages 5-6, Office Action C states:

> Regarding claim 20, Hotta et al. discloses a machine used for digital-to-analog conversion (fig. 1) comprising: a first counter (6) which provides a first count; means (the switch) for initializing the first count to a first digital number value (fig. 1); an analog reference source (8) which provides a first analog reference signal (fig. 1); means (9) for causing said first analog reference signal to change as a function of time (fig. 1); means [comparator](2) for detecting when the first count reaches a first digital threshold value (the comparator compares the digital value with a reference number; col. 3, lines 50-56); means for recording the value of the first analog reference signal as the first analog value when the first count reaches the first digital threshold value whereby the first analog value is the converted value of the first digital number value (col. 4, lines 19-27; abstract).

Hotta et al. column 3, lines 50-56 read as follows:

> An output signal SH (FIG. 2, (e)) of the sample and hold circuit 12 is applied to a comparator 2, and is compared with the ramp voltage Vr (FIG. 2, (g)). In synchronism with an output (FIG. 2, (h)) of the comparator 2 at the time when the ramp voltage has exceeded the output signal SH, an output (initial value: "0...0") of an m-bit counter 4 is set in a latch 51.

Hotta et al. column 4, lines 19-27 read as follows:

> In synchronism with the output of the comparator 2 at the time when the ramp voltage Vr has exceeded the sampled and held value, the content of the counter 4 is set in the latch 51. The content of the latch 51 is written to the address "0001" of the RAM 5 by a pulse corresponding to the succeeding first time interval of the compensating operation. The counter 6 counts up "1" more and its output becomes "0010".

Application claim **20** is an independent claim. Its dependent claims are claims **21-26**.

In numbered paragraph 20 on page 5 of Office Action C, there are the following errors in analysis and interpretation:

- The cited switch does not amount to means for initializing the first count to a first digital number value.
- The comparator does not detect when the first count reaches the first digital threshold value.
- There is no means for recording the value of the first analog reference signal.

Applicant will address these three issues below.

The cited switch does not amount to means for initializing the first count to a first digital number value

Office Action C asserts that with respect to Application claim **20**, Hotta et al. Fig. 1 comprises "means for initializing the first count to a first digital number value", identifying the means as a "switch", but not which one.

Hotta et al. Fig. 1 includes three explicit switches. They are switch **71**, switch **72**, switch **73**, and switch **74**. Switch **71** is connected to an output bus of first counter **6**, the counter identified by the Office Action as providing the first count, and to UB. Switch **72** is connected to LB and to "0". Switch **73** is connected to the output bus of RAM **5** and to "0".

As discussed in Hotta et al., when the circuits of Fig. 1 are operating in compensation calculation mode, first count values from counter **6** are passed to DAC **1** through switch **71**. Simultaneously, a "0" value is passed through switch **72** and through switch **73**. What DAC **1** sees as input, then, is a set of non-zero bits from switch **71** – in other words, the most-significant bits of an input – and also no non-zero least-significant bits and no correction term. So, for instance, if DAC **1** is a 16-bit converter, switch **71** might pass in the 6 most significant bits while the 10 least-significant bits and the correction

terms are both zero. Counter **6** then only has to count through 2^6 = 64 values, and RAM **5** need only have enough memory for 64 correction terms.

When the correction terms have been calculated and stored, DAC **1** can operate as a D/A converter. Its inputs are UB through switch **71**, LB through switch **72**, and the correction term from the RAM **5** OUT bus through switch **73**. Referring to the toy example again, UB would be the 6 most-significant bits, LB would be the 10 least-significant bits, and the correction term would be could have a designated number of bits stored in RAM **5** from counter **4**.

The three switches **71**, **72**, and **73** do not trigger initialization of counter **6**.

In the figure, the fourth switch is switch **74**. This switch determines whether the output of DAC **1** is passed to sample-and-hold circuit **12** or to sample-and-hold circuit **11**. The DAC **1** output is passed to sample-and-hold circuit **12** during computation of the correction terms, but is passed to the output O/P through sample-and-hold circuit **11** during compensated D/A conversion.

Switch **74** also does not trigger initialization of counter **6**.

There is therefore no switch depicted in Hotta et al. Fig. 1 which acts as "means for initializing the first count to a first count value".

The comparator does not detect when the first count reaches the first digital threshold value

Office Action C numbered paragraph 20 goes on to state that Hotta et al. Fig. 1 includes "means [comparator](2) for detecting when the first count reaches a first digital threshold value (the comparator compares the digital value with a reference number".

Examining Hotta et al. Fig. 1 as well as the cited text in Hotta et al. column 3 lines 50-56, it is clear that in fact comparator **2** compares two analog values – the sampled-and-held analog output of DAC **1**, and the voltage ramp Vr provided by ramp voltage generator **8**, which the Office Action is identifying as the first analog reference signal. Comparator **2**

does not compare a "digital value with a reference number" because it is not a digital comparator. It does not have a "digital threshold value" because both inputs are analog signals.

There is no means for recording the value of the first analog reference signal

Office Action C numbered paragraph 20 on pages 5-6 indicates that Hotta et al. Fig. 1 incorporates "means for recording the value of the first analog reference signal as the first analog value when the first count reaches the first digital threshold value whereby the first analog value is the converted value of the first digital number value".

However, referring to the text of Hotta et al. and Fig. 1, the first analog reference signal identified by Office Action C is the voltage ramp Vr provided by ramp voltage generator **8**. This signal is only provided to the inverting input of comparator **2**. Quite explicitly, there is no circuit shown to record an analog value of the voltage ramp.

Hotta et al. lacks all the limitations of claim 20

Applicant therefore submits that Office Action C numbered paragraph 20 mis-identified one of the four switches in Hotta et al. Fig. 1 as the element in part (b) of claim **20**. Applicant recognizes, of course, that counter **6** can be initialized, just not with the elements identified by Office Action C.

Further, Hotta et al. and its Fig. 1 fail to include or suggest either part (f) of claim **20** or part (g) of claim **20**.

Applicant therefore submits that Hotta et al. does not anticipate claim **20** and requests withdrawal of rejection under 35 USC 102 (b).

Office Action C – p. 6 – paragraph 21 – 35 USC 102(b) Rejection of Claim 21

In numbered paragraph 21 on page 6, Office Action C states:

> Regarding claim 21, Hotta et al. discloses a machine (fig. 1) further including: a second counter (4), which provides a second count; . means for initializing the second count to a second digital number value (fig. 1); means (9) for causing said second count to change as a function of time (fig. 1); means (2) for detecting when the second count reaches a second digital threshold value (fig. 1); means for recording the value of the first analog reference signal as the second analog value when the second count reaches the second digital threshold value whereby the first analog value is the converted value of the first digital number value and whereby the second analog value is the converted value of the second digital number value (col. 4, lines 19-27, abstract).

Application claim **21** is a dependent claim of independent claim **20**. As Applicant just discussed above, Hotta et al. lacks claim **20** elements (f) and (g). These elements are limitations of claim **21** as well.

Considering the additional discussion of Office Action C numbered paragraph 21, in fact:

- Comparator **2** does not constitute means for detecting when the second count reaches a second digital threshold value.
- Hotta et al. lacks any means for detecting when the second count reaches a second digital threshold value.
- Hotta et al. lacks any means for recording the value of the first analog reference signal as the second analog value when the second count reaches a second digital threshold value and whereby the second analog value is the converted value of the second digital number value.

Comparator 2 does not detect when the second count reaches a second digital threshold value

As discussed previously, comparator **2** is an analog comparator accepting as inputs only the analog ramp voltage Vr from ramp voltage generator **8** and the sample-and-held

analog output of DAC **1**. It is not a digital comparator and does not detect when the time-varying second count of counter **4** reaches a second digital threshold value.

Hotta et al. lacks any means for detecting when the second count reaches a second digital threshold value

Second counter **4** is free-running with respect to comparator **2**. The output of comparator **2** does control when latch **51** acquires a value of the second count from counter **4**, but the acquisition trigger depends on when voltage ramp Vr reaches the value of the sampled-and-held output of DAC **1** and not on the second count. In fact, there is no means for detecting when the second count reaches a second digital threshold value in Hotta et al., and there isn't even an identifiable second threshold value.

Hotta et al. lacks any means for recording the value of the first analog reference signal as the second analog value

Hotta et al. does not depict any means for recording the value of the analog reference signal, identified as the voltage ramp. There aren't means for recording a first value as discussed with respect to claim **21** parent claim **20**, and there also aren't means for recording a second value. Additionally, there is neither a second digital threshold value nor means for detecting when the second count would reach such a value.

Hotta et al. lacks all the limitations of Application claim 21

Applicant therefore submits that Hotta et al. lacks the following elements of Application claim **21**: parent claim **20** parts (f) and (g), and claim **21** parts (d) and (e). Applicant therefore submits that Hotta et al. does not anticipate claim **21**, and requests withdrawal of rejection under 35 USC 102(b).

Office Action C – pp. 6-7 – paragraph 22 – 35 USC 102(b) Rejection of Claim 22

In numbered paragraph 22 on pages 6-7, Office Action C states:

> Regarding claim 22, Hotta et al discloses a machine (fig.1), which the first digital threshold value is the same as the second digital threshold value (fig. 1).

Building on the above arguments for parent claims **20** and **21**, there is neither a first digital threshold value nor a second digital threshold value in Hotta et al. Fig. 1. Claim **22** includes all of the limitations of claims **20** and **21** with the additional requirement of the two digital threshold values being the same.

Applicant therefore submits that Hotta et al. does not anticipate claim **22** and requests withdrawal of 35 USC 102 (b) rejection.

Office Action C – p. 7 – paragraph 23 – 35 USC 102(b) Rejection of Claim 23

In numbered paragraph 23 on page 7, Office Action C states:

> Regarding claim 23, Hotta et al. discloses a machine (fig. 1) in which the first digital threshold value is equal to zero (col. 4, lines 33-35)

Column 4, lines 33-35 of Hotta et al. read as follows:

> the compensation is completed. At the completion of the compensation, the outputs of the counter **4** and the counter **6** are restored to the initial states "0...0" and "0000," and the flip-flop **3** is reset and the ramp voltage

The excerpt from column 4 of Hotta et al. states that after the calculation of the digital correction terms which are stored in SRAM **5** is complete, counters **4** and **6** are reset. In conjunction with numbered paragraph 23 of Office Action C, the implication seems to be that Office Action C interprets the first count and the second count to be equivalent to the first digital threshold value and the second digital threshold value, and that since the

counts can have a value of 0, Hotta et al. anticipates claim **23**. However, if the first count is identical to the first digital threshold level and the second count is identical to the second digital threshold level, then means for detecting when the two digital counts reach the two digital thresholds would be superfluous, as would means for recording analog signal values at those times.

In fact, as previously discussed, Hotta et al. lacks either a first digital threshold value or a second digital threshold value, detection means for determining when time-varying counts reach digital threshold values, and recording means for recording corresponding analog reference signal values. Since Hotta et al. fails to have a first digital threshold level, it fails also to have a first digital threshold level equal to zero.

Applicant therefore submits that Hotta et al. does not anticipate claim **23** and requests withdrawal of 35 USC 102 (b) rejection

Office Action C – p. 7 – paragraph 24 – 35 USC 102(b) Rejection of Claim 24

In numbered paragraph 24 on page 7, Office Action C states:

> Regarding claim 24, Hotta et al. discloses a machine (fig. 1) further including: a second counter (4) which provides a second count (fig. 1); second analog reference source (the input of the sampling circuit) which provides a second analog reference signal (fig. 1); means for initializing the second count to a second digital number value (fig. 1). Means (9) for causing the second count to change as a function of time (fig. 1); means for causing the second analog reference signal to change as a function of time (the clocking in the circuitry causes the analog reference signal to change in function of time);. Means (2) for detecting when the second count reaches a second digital threshold value (fig. 1); means for recording the value of the second analog reference signal as the second analog value when the second count reaches the second digital threshold value whereby said first analog value is the converted value of the first digital number value and whereby the second digital number value (col. 4, lines 19-27; abstract) [the sample-and-hold is used to record the value of the analog reference signal];

Application claim **24** is a dependent claim of independent claim **20**. As previously discussed, Hotta et al. lacks all the limitations of claim **20**. It therefore also lacks all the limitations of dependent claim **24**.

With respect to Office Action C numbered paragraph 24,

- The indicated second analog reference signal is itself just the D/A converter output.
- The clocking does not cause the analog reference signal to change as a function of time without a change in the D/A converter inputs.
- Comparator **2** does not detect when the second count reaches a second digital threshold value, and there are in fact no means for such detection or even such a digital threshold value.
- There are no means for recording the second analog reference value when the second count reaches the second digital threshold value.

The indicated second analog reference signal is itself just a D/A converter output

In numbered paragraph 24 on page 7, Office Action C identifies the output of DAC **1** as the second analog reference signal of Application claim **24**. However, this analog reference signal is itself just a D/A converter, while the invention is a D/A converter. There is no point to having all the elements of parent claim **20** and the additional elements in claim **24** with their corresponding limitations if a black-box D/A converter is available where one can just apply a desired digital input and get a desired analog output. Getting the analog output from the digital input is what the entire Application is all about.

The clocking does not cause the analog reference signal to change as a function of time without a change in the D/A converter inputs

The clock circuitry alone is insufficient to cause the second analog reference signal to change as a function of time. The actual digital inputs of DAC **1** also have to change. The second count of counter **4** is never applied directly to DAC **1**, and further, it's

possible for counter **4** to fully cycle during each value of the first count from counter **6** applied to DAC **1** during a correction calculation cycle. So in fact, there is absolutely no correspondence whatsoever between the value of the second count and the value of the output of DAC **1**. They are independent.

Comparator 2 does not detect when the second count reaches a second digital threshold value, and there are in fact no means for such detection or even such a digital threshold value

As previously discussed, comparator **2** is an analog comparator. Building on the suggestion of Office Action C numbered paragraph 24, comparator **2** compares the time-varying first analog reference signal Vr from ramp voltage generator **8** to the sampled-and-held output of DAC **1**, which is paragraph 24's sampled-and-held second analog reference signal. Comparator **2** does not detect when the second count from counter **4** reaches a second digital threshold value, and there aren't in Hotta et al. Fig. 1 or specification identifiable means for such comparison or an identifiable second digital threshold value.

There are no means for recording the second analog reference value when the second count reaches the second digital threshold value

Since there aren't either a second digital threshold value or detection means for determining when the second count reaches, well, any value at all, there is no way of determining the cited "when". As discussed above, the value of the second count and the value of the DAC **1** output are independent. Sample-and-hold circuits **11** and **12** can certainly record analog output values from DAC **1**. In fact, doing so is their principal purpose. They therefore represent "means for recording the second analog reference value" but fail to have the additional limitations in part (g) of claim **24**.

Hotta et al. does not anticipate claim 24

Hotta et al., in addition to lacking all the limitations of parent claim **20**, further lacks all the limitations in dependent claim **24**. Applicant therefore submits that Hotta et al. does

not anticipate claim **24** and requests withdrawal of claim **24** rejection under 35 USC 102(b).

Office Action C – p. 7 – paragraph 25 – 35 USC 102(b) Rejection of Claim 25

In numbered paragraph 25 on page 7, Office Action C states:

> Regarding claim 25, Hotta et al. discloses a machine (fig. 1) in which the digital first digital threshold value is the same as said second digital threshold value (fig. 1).

Applicant has already discussed that Hotta et al. lacks all the limitations of parent claims **20** and **24**. The further limitation of claim **25** is not depicted or suggested in Hotta et al. Therefore Applicant submits that Hotta et al. fails to have all the limitations of claim **25** and thus does not anticipate claim **25**. Applicant requests withdrawal of claim **25** rejection under 35 USC 102(b).

Office Action C – p. 7 – paragraph 26 – 35 USC 102(b) Rejection of Claim 26

In numbered paragraph 26 on page 7, Office Action C states:

> Regarding claim 26, Hotta et al. discloses a digital-to-analog converter (fig. 1) in which the first digital threshold is equal to zero (col. 4, lines 33-35).

Hotta et al. column 4, lines 33-35 read as follows:

> [At the completion of] the compensation, the outputs of the counter **4** and the counter **6** are restored to the initial states "0…0" and "0000," and the flip-flop **3** is reset and the ramp voltage [Vr is also restored to "0" by a carry signal CA of the counter **6**].

Hotta et al. are thus stating that when the portion of the circuit operation devoted to computing the digital correction terms is complete, counter **4**, counter **6**, and flip-flop **3** are reset. The count values are reset to "0".

Office Action C's implication is thus that the first digital threshold value is "0" and that the second digital threshold value is "0". However, based on Hotta et al's discussion, these "0" values are merely possible values of the two counts, notably the initial values provided when the counter circuits are reset. Hotta et al. still lacks all the limitations of parent claims **20**, **24**, and **25**, and so does not anticipate dependent claim **26**. Applicant requests withdrawal of claim **26** rejection under 35 USC 102(b).

Office Action C – pp. 7-8 – paragraph 27 – 35 USC 102(b) Rejection of Claim 27

In numbered paragraph 27 on pages 7-8, Office Action C states:

> Regarding claim 27, Hotta et al. discloses a digital-to-analog converter (fig.1) comprising a first circuit element (6) wherein the first circuit element (6) is used in a first instance for a first conversion of a first digital number to a first analog value (fig. 1) the first circuit element (6) is also used in the first instance for a second conversion of a second digital number to a second analog value (fig. 1) [note a the input of the DAC 1 there are the UB and LB that are used at a different time in the process to produce an analog signal at the output of the DAC 1]; the first circuit element (6) comprises a first parameter (the clock 9) that varies with time during a conversion operation whereby the first circuit element is effectively shared in the first conversion and in the second conversion, rather than used in said first instance for said first conversion and separately in a second instance for said second conversion, and whereby the first circuit element is not simply a constant reference signal.

Applicant's original intent with independent claim **27** is illustrated by Application Figures 2 and 3. Figure 2 has a shared analog reference source going to multiple sample-and-hold circuits, while Figure 3 has a shared analog reference source and a shared time-varying counter. See also the "whereby" clause at the end of claim **27**.

Office Action C reasoning is that in Hotta et al. counter **6** is a first circuit element used "in a first instance" for conversion of UB and "at a different time" for conversion of LB. In fact, there are only two modes of operation. In one mode – regular D/A conversion – DAC **1** has as input the digital number defined by UB and LB, as well as a digital correction term from the look-up table stored in RAM **5**. In the other mode – digital correction computation – first count values from counter **6** are supplied in place of UB and "0" strings are supplied in place of LB and the digital corrections. At no time is UB converted separately from LB. They're either both used simultaneously as, respectively, the upper (more significant) bits and the lower (less significant) bits of a digital number input for DAC **1**, or else both are not used. They are never used one without the other.

That they are depicted in Fig. 1 as passing through different switches is mainly to illustrate that DAC **1** can have N bits of precision, with only M < N bits of precision used for the counter. Input corrections are then computed and stored for a strict subset of all possible DAC **1** inputs.

The phrase "at a different time" in numbered paragraph 27 should be an immediate sign of differing instances. Any D/A converter without fixed inputs can be viewed as using its circuitry to convert one digital number input at one time and another, different digital number input at another time. In keeping with the concluding "whereby" clause of original claim **27**, conversions at different times should be viewed as separate instances. Similarly, two completely separate D/A converters operating either at different times or at the same time should also be viewed as separate instances.

Recognizing that the wording of original claim **27** was too broad and potentially confusing, Applicant has amended claim **27** to reflect both the simultaneous nature of the two conversions and the fact that the shared first circuit element can be a counter or an analog reference source. The change narrows claim **27** without introducing new material, as the reduced scope is clearly shown in Application Figs. 2 and 3 and also discussed in the specification.

Applicant submits that Hotta et al. does not anticipate the narrowed claim **27**, and therefore requests withdrawal of 35 USC 102(b) rejection of the claim.

Office Action C – p. 8 – paragraph 28 – 35 USC 102(b) Rejection of Claim 28

Applicant has amended claim **28** which depends on narrowed claim **27**. Applicant submits that Hotta et al. does not anticipate the narrowed claim **27**, and therefore requests withdrawal of 35 USC 102(b) rejection of claim **28**.

Office Action C – p. 8 – paragraph 29 – 35 USC 102(b) Rejection of Claim 29

In numbered paragraph 26 on page 7, Office Action C states:

Regarding claim 29, Hotta et al. discloses a digital-to-analog converter (fig. 1) further including: a first digital comparator (2) providing a first digital comparator output (fig. 1) . means for averaging said the digital comparator output over time whereby the digital-to-analog converter (1) can implement shared parallel pulse-width modulation digital-to-analog conversion (figs. 2, 4)

Application claim **29** was originally a dependent claim of both claims **27** and **28**. The two parent claims now cover a narrower scope consistent with Application's figures and specification.

Moreover, in Hotta et al. Fig. 1, comparator **2** is not a digital comparator, as previously discussed. It does provide a digital indicator signal indicating which input is greater than the other. However, Hotta et al. Fig. 1 does not include means for averaging a comparator output over time, and the specification does not suggest this. Nor, for that matter, do Hotta et al. Fig. 1, 2, 4, or the Hotta et al. specification discuss or suggest pulse-width modulation D/A conversion or shared pulse-width modulation D/A conversion.

With regard to Hotta et al. Fig. 2, only graph (h) shows the comparator output, which is clearly depicted as a step function and which is not in fact a digital comparator output, since comparator **2** accepts only analog inputs. With regard to Hotta et al. Fig. 4, only graph (c) shows the comparator output, which again is clearly depicted as consisting of perfect steps up and down. The non-step graphs (b), (c), (e), and (g) in Fig. 2 and (b) in Fig. 4 depict acquisition settling times of sample-and-hold circuits and output settling times of DAC **1**.

Applicant therefore submits that Hotta et al. fails to include all of the limitations of claim **29**. Applicant requests withdrawal of claim **29** rejection under 35 USC 102(b).

Office Action C – p. 8 – paragraph 30 – 35 USC 102(b) Rejection of Claim 31

In numbered paragraph 30 on page 8, Office Action C states:

Regarding claim 31, Hotta et al. discloses a digital-to-analog converter (fig. 1) in which the first circuit element (6) is a first analog reference source (fig. 1).

In Hotta et al. Fig. 1, circuit element **6** is a counter. This counter is not a first analog reference source. It is a digital number reference source.

Applicant has amended claim **31** to reflect the narrowing and clarifying language added to parent claim **27**. Applicant submits that Hotta et al. does not anticipate the narrowed claim **27**, and therefore requests withdrawal of 35 USC 102(b) rejection of claim **31**.

Office Action C – pp. 8-9 – paragraph 31 – 35 USC 102(b) Rejection of Claim 32

In numbered paragraph 31 on pages 8-9, Office Action C states:

> Regarding claim 32, Hotta et al. discloses a machine used for digital-to-analog conversion (fig. 1) , comprising: a first counter (6) which provides a first count (fig 1) . means for initializing said first count to a first digital number value (fig. 1); means (9) for causing the first count to change as a function of time (fig. 1); . means (2) for detecting when the first count reaches a first digital threshold value (fig. 1); means for averaging the output of the means for detecting when the first count reaches a first digital threshold whereby the output of the means for averaging is the converted value of said first digital number value (fig. 1).

Office Action C is again asserting that comparator **2**, an analog comparator with voltage ramp Vr and sampled-and-held values of the analog output of DAC **1** as inputs, is a digital comparator. Hotta et al. Fig. 1 lacks both means for detecting when the first count reaches a first digital threshold value and a digital threshold value. Moreover, it also lacks means for averaging any signal, analog or digital.

Hotta et al. lacks elements (d) and (e) of claim **32**. Applicant therefore submits that it does not anticipate claim **32** under 35 USC 102(b) and requests withdrawal of the claim rejection.

Office Action C – p. 9 – paragraph 32 – 35 USC 102(b) Rejection of Claim 33

In numbered paragraph 32 on page 9, Office Action C states:

> Regarding claim 33, Hotta et al. discloses a machine (fig. 1) means (2) for detecting when the first count reaches a first digital threshold value is a first digital comparator (fig. 1).

Numbered paragraph 32 states very directly the idea, expressed in numerous other parts of the 35 USC 102(b) rejection paragraphs of Office Action C, that comparator **2** in Hotta et al. Fig. 1 is a digital comparator. Comparator **2** is not a digital comparator. It is an analog comparator.

In the specification, Applicant repeatedly went to great lengths to define the inputs, output, and function of a digital comparator. Applicant was careful to use the phrase "digital comparator" rather than the ambiguous "comparator" or the specifically-different "analog comparator". Office Action C adopts a very broad interpretation of "digital comparator" and "comparator" which is unwarranted given Applicant's entirely reasonable attempts to avoid such confusion.

Again, comparator **2** in Hotta et al. Fig. 1 does not detect when the time-varying first count reaches a first digital threshold value. It detects when time-varying analog voltage ramp Vr reaches a held (and hence non-time-varying) analog output of DAC **1**. Hotta et al. does not have all of the limitations of claim **33** or of its parent claim **32**. Applicant submits that Hotta et al. thus does not anticipate claim **33** under 35 USC 102(b), and requests withdrawal of the rejection.

Office Action C – p. 9 – paragraph 33 – 35 USC 102(b) Rejection of Claim 34

In numbered paragraph 33 on page 9, Office Action C states:

> Regarding claim 34, Hotta et al. discloses a machine (fig. 1) in which said first digital threshold level is zero, whereby no storage means are necessary to hold the value of the first digital threshold level and whereby the means (2) for detecting when the first count reaches the first digital threshold level can be implemented with simple digital logic such as a single multiple-input AND gate (30) [fig. 1].

Claim **34** is dependent on claim **32**, and has all the limitations of its parent claim. As discussed above, Hotta et al. does not have all the limitations of claim **32**. Further, there is no evidence that Hotta et al. Fig. 1 or its specification has or suggests a digital threshold level, that such a level would be zero, or that storage means would or would not be required for a zero digital threshold level. Moreover, the final statement of numbered paragraph 33 asserts that comparator **2** in Hotta et al. Fig. 1 incorporates AND gate **30**. Aside from this clearly not being the case, there is nothing to indicate or suggest any sort of digital logic internal to comparator **2**, especially considering that it is an analog comparator.

Applicant therefore submits that Hotta et al. does not anticipate claim **34**, and requests withdrawal of 35 USC 102(b) rejection of the claim.

Claim Rejections – 35 USC SS 103

In numbered paragraph 35 on page 9, Office Action C states:

> Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hotta et al. in view of Sakuragi (US Patent Number 6,542,105).

Calendar issues noted

Application filing date is February 28, 2002.

Hotta et al. issue date is April 26, 1983. The US filing date is October 8, 1980. Foreign application priority filing in Japan is listed as October 24, 1979.

Sakuragi (US Patent 6,542,105) has an issue date of April 1, 2003. Sakuragi has an initial filing date of December 13, 2001. Sakuragi issue date is thus a full year after Application filing date, while Sakuragi filing date is less than three months prior to Application filing date.

Reasoning in Office Action C

In numbered paragraph 36 on pages 9-10, Office Action C supports 35 USC 103(a) rejection of claim **30** as anticipated by Hotta et al. in view of Sakuragi as follows:

> Regarding claim 30, Hotta et al. does not specifically disclose an analog-to-digital converter comprising a digital-to-analog converter, whereby parallel analog-to-digital conversion of a multiplicity of analog values to a multiplicity of digital number values can share a circuit element (counter) [1] (fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hotta et al.'s system with that of Sakuragi in order to enhance an ADC speed while maintaining the ADC conversion.

Sakuragi's invention is a modification of a basic single-slope A/D converter. In contrast to the past when a constant current charging a capacitor would be used to generate the

reference ramp, a D/A converter is used to generate a staircase ramp (see Sakuragi Fig. 2). The problem with using a D/A converter to generate the analog reference ramp is that in the intended application environment – A/D conversion in an imaging system with massive numbers of sensors – the settling time for the D/A converter limits the A/D conversion rate. Sakuragi's contribution is to run through the digital count sequence quickly, ignoring that the D/A converter output hasn't settled, until such time as the D/A converter output is sufficiently close to the unknown analog input of the A/D converter. The count speed is then reduced and the D/A converter outputs are allowed to settle.

The fundamental idea of Sakuragi – running the count and reference generation quickly when the reference and unknown analog signals are far apart and slowly when they're close – teaches away from shared parallel A/D conversion. The clear target is fast serial A/D conversion, not shared parallel A/D conversion. In the serial form, faster overall throughput (e.g. conversions per second) is achieved by shortening each individual conversion operation. Each individual conversion operation is sped up by foregoing settling accuracy when it is not needed.

Insofar as Sakuragi addresses parallel A/D conversion, each converter instance has one counter, one comparator, and one component D/A converter, and parallelism comes from separate instances of Sakuragi A/D converters. The components are not shared. See Sakuragi Fig. 11, which depicts a sensor array. The sensor cells are arranged in rows and columns. The sensor outputs from each column are applied to a single instance of the variable-count-rate A/D converter which is Sakuragi's main invention. Within a column, the A/D conversion is serial, but there are parallel – and completely separate – Sakuragi A/D converters operating on the various columns.

The only part of Sakuragi which describes parallel A/D conversion with shared components is Fig. 14, which Sakuragi identifies as prior art on which Sakuragi ideas attempt to improve.

Combination of Hotta et al. with Sakuragi

The invention of Hotta et al. is a D/A converter (DAC **1** in Fig. 1) with additional circuitry (most of the remaining circuitry in Fig. 1) for computing a look-up table of digital

correction terms which are used to modify the digital number inputs of the converter in order to compensate for non-linear behavior of the converter's output.

One reason why one wouldn't combine the invention of Hotta et al. with the invention of Sakuragi is that Hotta et al.'s invention is presently 22 years old by issue date, 25 years old by filing date, and either way from a time when it was quite difficult to make a suitably linear D/A converter. Hotta et al. teaches taking a D/A converter with poor transfer function linearity and modifying it to have improved transfer function linearity, in a way which relies on a relatively slow compensation cycle. In the intervening 25 years, advances in semiconductor technologies have made it much easier to design a D/A converter that is both inherently fast and with good transfer function linearity – in other words, a better DAC **1** black box of Hotta et al. Fig. 1 that obviates the need for the elaborate compensation-calculation circuitry.

However, if one were to combine Hotta et al. with Sakuragi, what one would get is Hotta et al. DAC **1** and its associated circuitry from Fig. 1 inserted in place of Sakuragi element D/A converter **2**. Whether the insertion takes place in Sakuragi Fig. 1, Fig. 11, or Fig. 14, the Hotta et al. linearized-output D/A converter is used to generate one analog reference waveform at a time – in other words, for one D/A conversion at a time. There is no shared parallel D/A conversion suggested or implied.

Note that Applicant has narrowed parent claim **27** of claim **30** so that both claims match the material discussion of the Application's specification and figures. With the narrowing language, claim **30** now has the specific claim limitation of an A/D converter comprising the D/A converter of claim **27** having a shared, simultaneously-used first circuit element which is the counter for two simultaneous D/A conversions or the analog reference source for two simultaneous D/A conversions.

Applicant therefore submits that the combination of Hotta et al. and Sakuragi fails to have or suggest all of the limitations of claim **30**, and requests withdrawal of 35 USC 103(a) rejection of claim **30**.

Regarding Allowable Subject Matter discussion in Office Action C

Office Action C indicated allowability of claim **8** pending revision to incorporate the limitations of claim **1**, which had been rejected under 35 USC 102(b) as anticipated by Hotta et al. Applicant has persuasively argued in this Amendment C that, in fact, claim **1** is not anticipated by Hotta et al. because the latter fails to include or suggest all of the limitations in claim **1**. Applicant therefore submits that claim **8** does not need revision.

Office Action C stated the following in numbered paragraph 39 on page 10:

> Claims 2, 12-18 will be objected as claims having allowable subject matter upon complying to the 112, 1st rejection above.

Applicant has addressed 35 USC 112 rejection of claims 2 and 12-18 with this Amendment C, but does not understand what paragraph 39 means, and requests clarification.

Conclusion

The Applicant submits that the specification and the claims are now in proper form, and that the claims are all patentable over the prior art. Therefore, the Applicant submits that this application is now in condition for allowance, which action is respectfully solicited.

Conditional Request for Constructive Assistance

The Applicant has amended the specification and claims of this application so that they are proper, definite, and define novel structure which is also unobvious. If, for any reason this application is not believed to be in full condition for allowance, the Applicant, an independent inventor and pro se filer, respectfully requests the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P § 2173.02 and § 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very Respectfully,

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Certificate of Mailing: I hereby certify that this correspondence, and attachments, if any, will be deposited with the United States Postal Service by First Class Mail, postage prepaid, in an envelope addressed to "Mail Stop Non-Fee Amendments, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below.

October 27, 2005 Charles Douglas Murphy

Charles Douglas Murphy, Applicant